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EXAMINER	
SHRADER, LAWRENCE J	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Supplemental Office Action Summary

Application No. 09/679,434	**Applicant(s)** DAMRON ET AL.	
Examiner Lawrence Shrader	**Art Unit** 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)□ This action is **FINAL**. 2b)☒ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3 and 10* is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-20* is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) □ Notice of Informal Patent Application (PTO-152)

6) □ Other: _____.

DETAILED ACTION

1. This supplemental office action includes the rejections of new claims 19 and 20, which were inadvertently omitted in the previous office action.

2. The arguments put forth by the Applicant in the Amendment filed on April 23, 2004 have been fully considered, but are moot in view of the new grounds of rejection. Claims 3 and 10 have been cancelled, and claims 1, 2, 4 – 9, 11 – 18 remain rejected, and claims 19 and 20 are new.

Claim Rejections - 35 USC § 112

3. The rejection of claim 3c under the second paragraph of 35 U.S.C. 112 is withdrawn in view of the amendments filed on April 23, 2004.

Oath/Declaration

4. The declaration filed on 10/03/2000 is acknowledged. However, the Applicant must disclose information material to patentability under 37 C.F.R. 1.56, not a portion of 37 C.F.R. 1.56 (in this case 1.56a). See 37 C.F.R. 1.63, which states the declaration must "state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56." A new oath/declaration is required.

Specification

5. The objection to the Abstract because the length exceeds 150 words is withdrawn in view of the amendment filed on April 23, 2004.

6. The updating of the serial number information of the related applications disclosed on page 1 of the specification is acknowledged.

7. The objection to claims 4, 11, and 12 because of incorrect numbering/lettering is withdrawn in view of the amendment filed on April 23, 2004.

8. Newly amended claims 5, 12, and 15 are objected to because of the following informalities:

Amended claims 5 and 12 both have two steps labeled (hi1); also claim 15 has two step (c3)'s, therefore claim 15 should be re-lettered with steps (e1) through (e5).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2, 7; 8, 9, 14, 15; and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasbold et al., U.S. Patent 5,202,975, and further in view of Joffe, U.S. Patent 5,901,147.

In regard to claim 1:

Rasbold discloses a scheduler with a method for ordering instructions:

"(a) determining dependencies between instructions in said plurality of instructions;"

Rasbold discloses the determining of dependencies at column 2, lin55 – 58.

"(b) creating a directed acyclic graph showing said dependencies in said plurality of instructions, where said directed acyclic graph's nodes each correspond to an instruction from said plurality of instructions;"

Rasbold discloses the creation of a directed acyclic graph (DAG) where the nodes correspond to one of a plurality of instructions (column 8, lines 59 – 62; column 3, lines 16 – 20; e.g., Figure 2)

"(c) identifying one or more queues, including a first queue;"

Rasbold discloses the creation of at least one queue (column 2, lines 1 – 6).

"(d) traversing said directed acyclic graph in a dependency-preserving manner;"

Rasbold discloses traversing the directed acyclic graph in a dependency-preserving manner (column 2, lines 55 – 58; column 3, lines 15 – 29).

"(e) creating a ready set of nodes comprising nodes in said directed acyclic graph having corresponding instructions in a ready state;"

Rasbold discloses a ready set of instructions (corresponding to the DAG nodes) that are scheduled for issuance (column 4, lines 20 – 27; column 9, lines 50 – 65).

"(f) finishing if there are no nodes having corresponding instructions in a ready state;"

Rasbold discloses that the scheduling is finished when the ready set has no more instructions (nodes) to process (column 10, lines 24 – 29).

> *"(g) identifying a threshold level in said first queue, said threshold corresponding to a maximum desirable fullness of said first queue;"*

Rasbold discloses the addition of instructions into a queue that wait to be issued to a processor (column 2, lines 1 – 6; figure 3 refs. 46 – 50), but does not disclose identifying a threshold level corresponding to maximum fullness. However, Joffe discloses a method of identifying and controlling thresholds of queues based on fullness of the queue (column 1, lines 21 – 32, 37 - 41). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold invention with the threshold identification and control as taught by Joffe because the maximum threshold is useful for controlling memory usage as taught by Joffe at column 1, lines 24 – 26.

> *"(h) if said first queue is less full than said threshold, choosing a node in said ready set that corresponds to an instruction that would increase the fullness of said queue, if any such node exists in said ready set;"*

Rasbold discloses a queue that issues instructions (corresponding to a DAG node) at column 2, lines 1 – 6. Also, disclosed at column 4, lines 51 – 60 is that instructions in the ready set are scheduled for execution, therefore the ready set satisfies the needs of the scheduling queue, but does not disclose identifying a threshold level corresponding to maximum fullness. However, Joffe discloses a method of identifying and controlling thresholds of queues based on fullness of the queue (column 1, lines 21 – 32, 37 - 41).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold invention with the threshold identification and control as taught by Joffe because the maximum threshold is useful for controlling memory usage as taught by Joffe at column 1, lines 24 – 26.

> *"(i) if said first queue is at least as full as said threshold, choosing a node in said ready set that corresponds to an instruction that would decrease the fullness of said queue, if any such node exists in said ready set;"*

Rasbold discloses the identification of an instruction that must have its issuance delayed (subtracted from an ordering) by pushing (enqueueing) the issuance of the instruction back in order (that is back in some form of queue) allowing another instruction that will benefit from early issuance to be moved to the ready set (column 4, lines 51 – 60), but does not disclose a threshold based on fullness of the queue. However, Joffe discloses a method of identifying and controlling thresholds of queues based on fullness of the queue (column 1, lines 21 – 32, 37 - 41). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold invention choosing a node from the ready set with the threshold identification and control as taught by Joffe because the maximum threshold is useful for controlling memory usage as taught by Joffe at column 1, lines 24 – 26.

> *"(j) if no node is chosen in (h) or (i), heuristically choosing a node in said ready set;"*

Rasbold discloses that if an instruction (corresponding to a node) is heuristically chosen if it can benefit form an early execution when another instruction issuance is delayed; it is moved to the ready set to "bubble" to the top of instructions to be scheduled (column 4, lines 51 – 60).

"(k) removing said chosen node from said directed acyclic graph;"

See Figure 4, ref. 48 of Rasbold and the accompanying text at column 10, lines 14 - 23.

"(1) modifying said first queue in accordance with said chosen node and its corresponding instruction;"

Rasbold discloses a queue issuing instructions (corresponding to a DAG node) at column 2, lines 1 – 6. The ready instructions are scheduled in the queue (see Figure 4, ref. 46) as new instructions enter or are shifted (modifying the queue) as disclosed at step (j) above.

"(m) modifying the order of instructions in said code file in accordance with said chosen node and its corresponding instruction; and,"

Rasbold discloses that if an instruction (corresponding to a node) is heuristically chosen if it can benefit form an early execution when another instruction issuance is delayed; it is moved to the ready set to "bubble" to the top of the queue of instructions to be scheduled (column 4, lines 51 – 60).

"(n) continuing processing at (d)."

See Figure 4 of Rasbold.

In regard to claim 2, incorporating the rejection of claim 1:

"...wherein:

said first queue is configured to facilitate scheduling of the instructions;"

Rasbold discloses the creation of at least one queue to facilitate scheduling (column 2, lines 1 – 6).

"said node chosen in (h) corresponds to an instruction that will add an element to said first queue;"

Rasbold discloses a queue that issues instructions (corresponding to a DAG node) at column 2, lines 1 – 6. Also, disclosed at column 4, lines 51 – 60 is that instructions in the ready set are scheduled for execution, therefore the ready set satisfies the needs of the scheduling queue.

"said chosen in (i) corresponds to an instruction that will remove at least one element from said first queue."

Rasbold discloses the identification of an instruction that must have its issuance delayed (subtracted from an ordering) by pushing (enqueueing) the issuance of the instruction back in order (that is back in some form of queue) allowing another instruction that will benefit from early issuance to be moved to the ready set (column 4, lines 51 – 60)

In regard to claim 7, incorporating the rejection of claim 1:

> *"...wherein said)l) comprises:*
>
> *(a) adding an element corresponding to said chosen node to said first queue if said first queue is less full than said threshold;"*

Rasbold discloses the addition of instructions into a queue that wait to be issued to a processor (column 2, lines 1 – 6). Also see Figure 3 refs. 46 – 50, but does not disclose a threshold based on fullness of the queue. However, Joffe discloses a method of identifying and controlling thresholds of queues based on fullness of the queue (column 1, lines 21 – 32, 37 - 41). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold invention choosing a node from the ready set with the threshold identification and control as taught by Joffe because the maximum threshold is useful for controlling memory usage as taught by Joffe at column 1, lines 24 – 26.

> *"(b) removing at least one element in accordance with said chosen node from said first queue if said first queue is at least as full as said threshold."*

Rasbold discloses the identification of an instruction that must have its issuance delayed (subtracted from an ordering) by pushing the issuance of the instruction back in order (that is back in some form of queue) allowing another instruction that will benefit from early issuance to be moved to the ready set (column 4, lines 51 – 60), but does not disclose a threshold based on fullness of the queue. However, Joffe discloses a method of identifying and controlling thresholds of queues based on fullness of the queue (column 1, lines 21 – 32, 37 - 41). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold invention choosing a node from the ready set with the threshold identification and control as taught by Joffe because the maximum threshold is useful for controlling memory usage as taught by Joffe at column 1, lines 24 – 26.

In regard to claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 1 (a corresponding method).

In regard to claim 9, incorporating the rejection of claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 2 (a corresponding method).

In regard to claim 14, incorporating the rejection of claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 7 (a corresponding method).

In regard to claim 15:

> *"A queue modeling instruction scheduler apparatus for use in compiling a program, the apparatus executable in a device having a processor operatively coupled to a memory, the apparatus comprising:*
>
> *(a) a directed acyclic graph creation module configured to:*
>
> *(a1) determine dependencies between instructions in a program to be compiled;*
>
> *(a2) create a directed acyclic graph showing said dependencies in said program, wherein said directed acyclic graph's nodes correspond to instructions in said program;"*

An apparatus corresponding to the method of claim 1. Rasbold discloses the creation of a directed acyclic graph (DAG) where the nodes correspond to one of a plurality of instructions (column 8, lines 59 – 62; column 3, lines 16 – 20; e.g., Figure 2).

> *"(b) a directed acyclic graph traversal and ready set identification module configured to:*
>
> *(b1) traverse said directed acyclic graph in a dependency-preserving manner;*
>
> *(b2) create a ready set of nodes;"*

An apparatus corresponding to the method of claim 1. Rasbold discloses traversing the directed acyclic graph in a dependency-preserving manner (column 2, lines

55 – 58; column 3, lines 15 – 29). Rasbold also discloses a ready set of instructions (corresponding to the DAG nodes) that are scheduled for issuance (column 4, lines 20 – 27; column 9, lines 50 – 65).

> *"(c) a ready set evaluation module configured to:*
>
> *(c1) identify which nodes in said ready set correspond to which instructions in said program;*
>
> *(c2) evaluate said instructions for their effect on memory operations;"*

An apparatus corresponding to the method of claim 1. Rasbold also discloses a ready set of instructions (corresponding to the DAG nodes) that are scheduled for issuance (column 4, lines 20 – 27; column 9, lines 50 – 65).

> *"(d) a queue management module configured to:*
>
> *(d1) manage at least one queue, where managing a queue comprises adding and removing elements from said at least one queue where said elements correspond to nodes from said directed acyclic graph;"*

An apparatus corresponding to the method of claim 1. Rasbold discloses the addition of instructions into a queue that wait to be issued to a processor (column 2, lines 1 – 6). Also see Figure 3 refs. 46 – 50. Rasbold discloses the identification of an instruction that must have its issuance delayed (subtracted from an ordering) by pushing (enqueueing) the issuance of the instruction back in order (that is back in some form of queue) allowing another instruction that will benefit from early issuance to be moved to the ready set (column 4, lines 51 – 60).

> *"(e) a code scheduling module operably connected to said program, said directed acyclic graph traversal and ready set identification module, said ready set evaluation module, said queue management module and said directed acyclic graph, wherein said code scheduling module is configured to:*

(e1) add and remove nodes from said directed acyclic graph;

(e2) determine and correlate a maximum desirable number of elements identifier for said at least one queue;

(e3) choose one of said nodes in said ready set that will change the number of elements in said at least one queue in accordance with said correlated identifier;

(e3) have elements of said at least one queue added and removed;

(e4) change the order of instructions in said program in accordance with said instructions, said nodes, and said at least one queue."

An apparatus corresponding to the method of claim 1. Rasbold discloses a queue issuing instructions (corresponding to a DAG node) at column 2, lines 1 – 6. The ready instructions are scheduled in the queue (see Figure 4, ref. 46) as new instructions enter or are shifted (modifying the queue) as disclosed at step (1i) above. Rasbold discloses that if an instruction (corresponding to a node) is heuristically chosen if it can benefit form an early execution when another instruction issuance is delayed; it is moved to the ready set to "bubble" to the top of the queue of instructions to be scheduled (column 4, lines 51 – 60).

In regard to claim 19:

(a) constructing a directed acyclic graph depicting dependencies among instructions in the set of instructions, wherein each node in the graph corresponds to an instruction in the set of instructions;

(b) identifying a ready set of nodes representing instructions having no dependencies on other instructions;

> *(c) identifying a target level of fullness within a queue configured to facilitate reordering of the set of instructions;*
>
> *(d) if the queue is less full than said target level:*
>
> > *(d1) selecting a node in said ready set that corresponds to an instruction that would generate a memory operation; and*
> >
> > *(d2) if said ready set includes no such node, heuristically selecting a node in said ready set;*
>
> *(e) if the queue is at least as full as said target level:*
>
> > *(e1) selecting a node in said ready set that corresponds to an instruction that requires completion of a previous memory operation; and*
> >
> > *(e2) if said ready set includes no such node, heuristically selecting a node in said ready set;*
>
> *(f) removing the selected node from the ready set and the graph; and*
>
> *(g) scheduling the instruction corresponding to the selected node."*

Claim 19 is rejected for the same corresponding reasons for the corresponding limitations of claim 1.

11. Claims 4, 5; 11, 12; 16, 17; and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasbold et al., U.S. Patent 5,202,975 as applied to claim 1 above, and further in view of Eickemeyer et al., U.S. Patent 5,377,336 (hereinafter referred to as Eickmeyer).

In regard to claim 4, incorporating the rejection of claim 1:

> *"...wherein said (c) comprises identifying a load queue, a prefetch queue, and a store queue, the method further comprising:*

> *"(aa) determining and correlating a maximum desirable number of elements for each of said load queue, said prefetch queue, and said store queue;"*

Rasbold discloses the creation of at least one queue (column 2, lines 1 – 6), which is used as a prefetch queue to keep instructions operating at the fastest and most efficient order (column 2, lines 46 – 51), but does not explicitly disclose a load and store queue, nor determine and correlate a maximum desirable number of elements identifier for each queue. However, Eickemeyer discloses both a load queue, with the number of entries (elements) in the queue determined by identifying performance and cost trade-offs (maximum desirable number of elements (column 8, lines 30 - 33); and a store queue (column 11, lines 19 – 55). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues, as well as identifying the maximum number of element in each queue as taught by Eickemeyer, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

> *"(bb) determining a precedence ordering between said load queue, said prefetch queue, and said store queue;"*

Rasbold discloses the creation of at least one queue (column 2, lines 1 – 6), which is used as a prefetch queue to keep instructions operating at the fastest and most efficient order (column 2, lines 46 – 51), but does not explicitly disclose a load and store queue. However, Eickemeyer discloses both a load queue, and a store queue (column 11, lines 19 – 55); as well as a precedence ordering illustrated at column 10. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues taught by Eickemeyer having precedence ordering, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

In regard to claim 5, incorporating the rejection of claim 1:

> *"...wherein said (c) comprises:*
>
> *(c1) determining a number of queues to use in accordance with a target processor;"*

Rasbold discloses determining which number of queues to use in accordance with a target processor, e.g., a pipelined scalar/vector processor (column 5, lines 40 – 64).

> *"(c2) determining a maximum desirable fullness for each of said determined number of queues;*

Rasbold discloses the use of a queue, but does not disclose a determining or coupling of an identifier for the maximum number of elements. However, Eickemeyer discloses both a load queue, with the number of entries (elements) in the queue determined by identifying performance and cost trade-offs (maximum desirable number of elements (column 8, lines 30 - 33); and a store queue (column 11, lines 19 – 55). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues, as well as identifying the maximum number of element in each queue as taught by Eickemeyer, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

> *"(c3) determining a precedence ordering between each of said determined number of queues;"*

Rasbold discloses the creation of at least one queue (column 2, lines 1 – 6), which is used as a prefetch queue to keep instructions operating at the fastest and most efficient order (column 2, lines 46 – 51), but does not disclose a precedence ordering between queues. However, Eickemeyer discloses a precedence ordering illustrated at column 10. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues taught by Eickemeyer having precedence ordering, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

Each of said (h) and said (i) comprises:

> *"(hi1) choosing one of said nodes in said ready set that will change the number of elements in one of said determined number of queues, in accordance with said precedence order and said maximum desirable fullness, if one of said nodes can be found; and,"*

Rasbold discloses the identification of an instruction (node) in the ready set that must have its issuance delayed (subtracted from an ordering – changing the number of elements) by pushing (enqueueing) the issuance of the instruction back in order (that is back in the prefetch queue) allowing another instruction that will benefit from early issuance to be moved to the ready set (column 4, lines 51 – 60), with the number of entries (elements) in the queue determined by identifying performance and cost trade-offs (maximum desirable number of elements (column 8, lines 30 - 33), but does not disclose a precedence ordering of queues. However, Eickemeyer discloses a load queue, and a store queue (column 11, lines 19 – 55) with a precedence ordering illustrated at column 10. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues taught by Eickemeyer having precedence ordering and maximun queue element identifiers, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

> *"(hi1) choosing one of said nodes in said ready set that will not change the number of elements in one of said determined number of queues, in accordance with said precedence order and said maximun desirable fullness, if none of said nodes in said ready set can be found that will change the number of elements in one of said determined number of queues."*

Rasbold discloses choosing an instructions when scalar interlocks are cleared, which would not change the number of elements in one of said queues (column 11, lines 66 – 67), having the number of entries (elements) in the queue determined by identifying performance and cost trade-offs (maximum desirable number of elements (column 8, lines 30 - 33), but does not disclose a precedence order. However, Eickemeyer discloses a load queue, and a store queue (column 11, lines 19 – 55) with a precedence ordering illustrated at column 10. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the instruction queue as taught by Rasbold with load and store queues taught by Eickemeyer having precedence ordering, because one would be motivated to decrease the overall execution time of Rasbold with more efficient loading and storing as taught in the Eickemeyer Abstract.

In regard to claim 11, incorporating the rejection of claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 4 (a corresponding method).

In regard to claim 12, incorporating the rejection of claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 5 (a corresponding method).

In regard to claim 16, incorporating the rejection of claim 15:

Claim 16 (an apparatus) is rejected for the same corresponding reasons put forth in the rejection of claim 4 (a corresponding method).

In regard to claim 17, incorporating the rejection of claim 15:

Claim 17 (an apparatus) is rejected for the same corresponding reasons put forth in the rejection of claim 5 (a corresponding method).

In regard to claim 20, incorporating the rejection of claim 19:

> *"...wherein: said instruction that would generate a memory operation comprises one of: a load, a prefetch and a store; and*
>
> *said instruction that requires completion of a previous memory operation is an instruction dependent upon one or more of: a load, a prefetch and a store."*

Claim 20 is rejected for the same corresponding reasons for the corresponding limitations of claim 4.

12. Claims 6, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasbold et al., U.S. Patent 5,202,975 as applied to claim 1 above, and further in view of Gutpa et al., U.S. Patent 5,941,983 (hereinafter referred to as Gupta).

In regard to claim 6, incorporating the rejection of claim 1:

> *"...where said ordering of said instructions in said code file uses a hardware scheduler in accordance with said chosen node and its corresponding instruction."*

Rasbold does not disclose a hardware scheduler, but Gupta discloses a hardware scheduler (column 2, lines 10 – 12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the Rasbold scheduler with invention with the hardware scheduler of Gupta because the modification provides a means to prevent instructions that are not ready from stalling the machine as taught by Gupta at column 2, lines 55 – 58.

In regard to claim 13, incorporating the rejection of claim 8 (a storage device), it is rejected for the same corresponding reasons put forth in the rejection of claim 6 (a corresponding method).

In regard to claim 18, incorporating the rejection of claim 15:

Claim 18 (an apparatus) is rejected for the same corresponding reasons put forth in the rejection of claim 6 (a corresponding method).

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence Shrader
Examiner
Art Unit 2124

13 July 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100